Buck Converter IC Circuit Analysis Sample Report

(Only selected portions are shown)

DEVICE	1000-mA, X-MHz HIGH-EFFICIENCY STEP-DOWN CONVERTER
Model Number	XXXXX
Maker	XXXXX
Package Marking	XXXXX
Chip Marking	1.29mm × 0.93mm = 1.20mm^2
Chip Size	3Metal-2Poly
Process	

IMPORTANT NOTICE

This report, request for investigation, or analysis is intended to assist our client in product development. This report is copyright protected by LTEC Corporation. Our intention is to provide accurate and reliable information to our customer. While we always aim for maximum precision, an absolute accuracy of all contents in this report cannot be guaranteed.
If contents of this report are used in patent infringement disputes, Ltec cannot accept any liability resulting from potential inaccuracies contained in this report.

Contact in the USA:
LTEC Corporation US Representative Office
2280 Zanker Road No: 203
San Jose CA 95134

Phone: (408) 432-7247
Website: www.ltecusa.com
Contact: info@ltecusa.com

Headquarters:
LTEC Corporation
42-8, 4-chome, Higashiarioka, Itami-city, Hyogo, Japan

Table of Contents

Table1 Chip Information

Product	XA, X-MHz HIGH-EFFICIENCY STEP-DOWN CONVERTER
Model Number	XXXXX
Maker	XXXXX
Package Type	6-pin CSP
Package Marking	XXXXX
Chip Marking	XXXXX
Chip Size	1.29mm X 0.93mm = 1.20mm^2
Process	3Metal-2Poly
Process Type	BiCMOS
Gate Length	0.5um

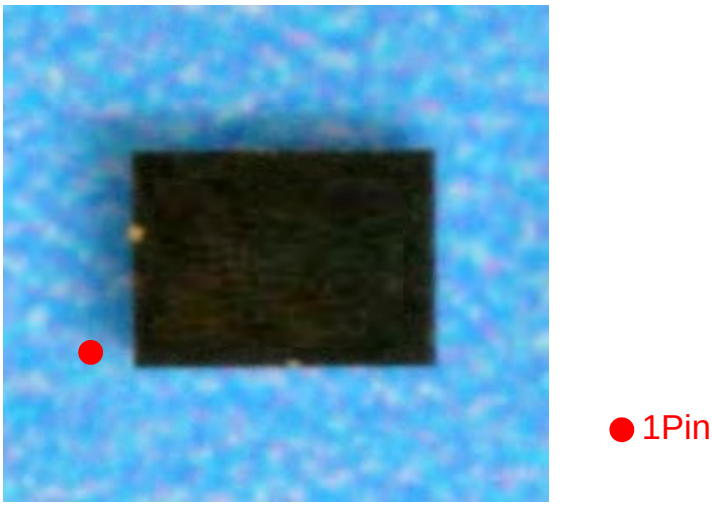


Photo.1-1 Package (Top View)

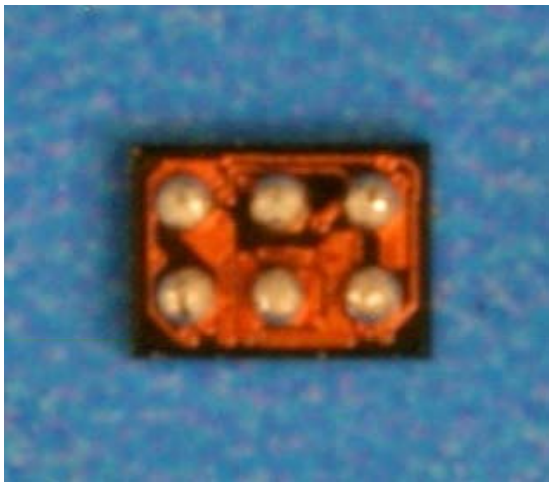
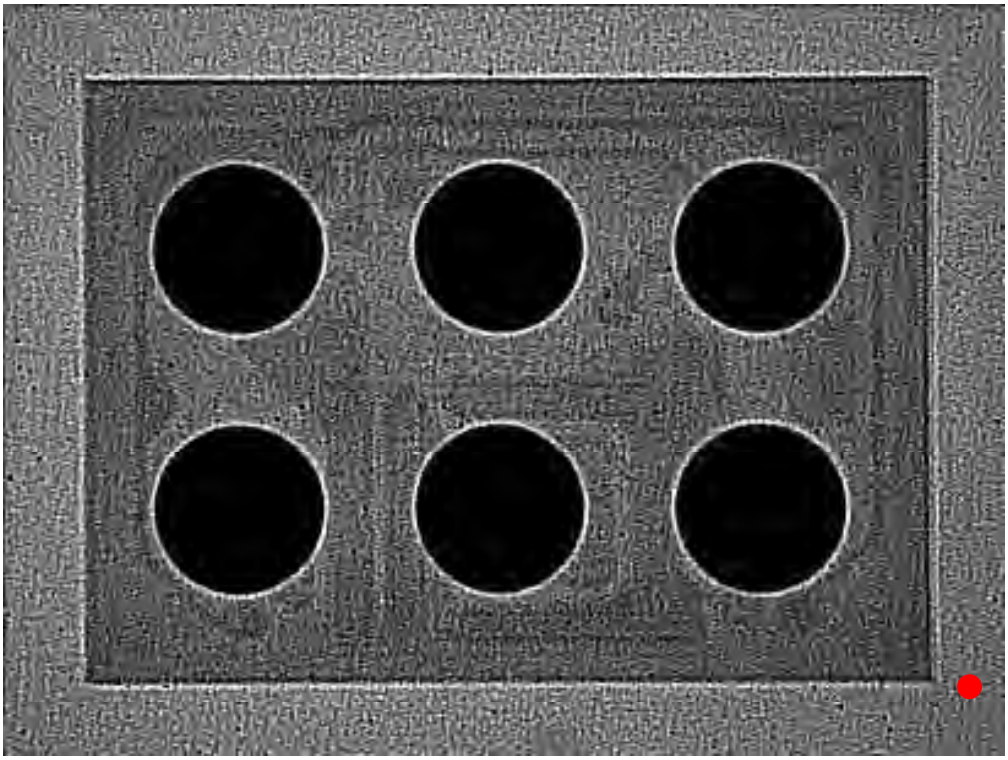


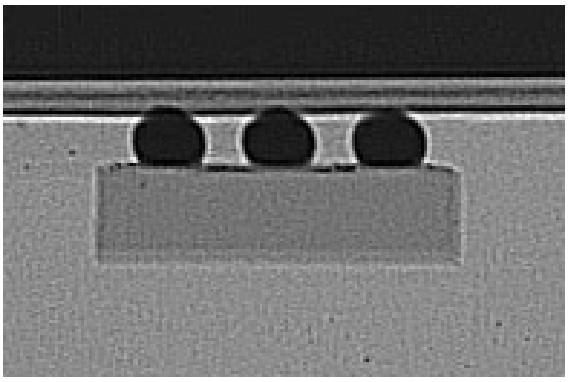
Photo.1-2 Package (Bottom View)



● 1Pin

（Bottom View）

Side View



（Side View）

Photo.2 X-Ray

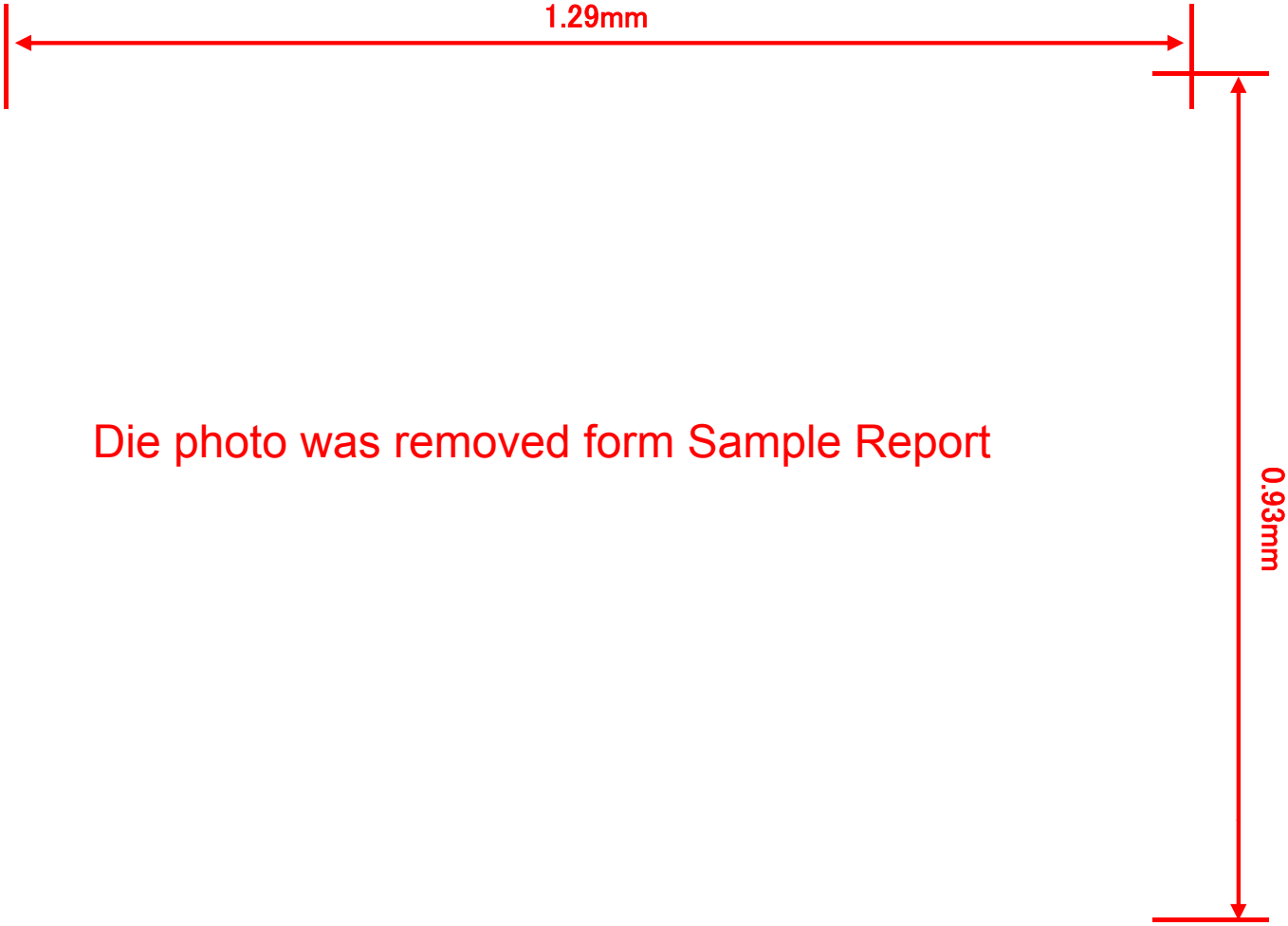


Photo.3-1 Chip Overview

1

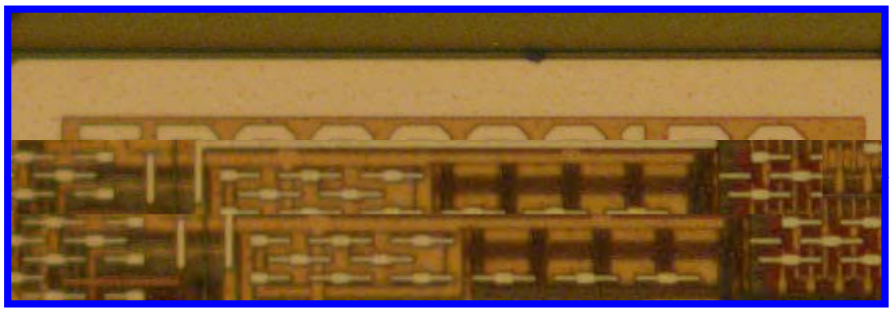


Photo.3-2 Chip Marking1

2

Photo.3-3 Chip Marking2

Pin assignment was removed from Sample Report

Photo.4-1 Pin Assignment (Bottom View)

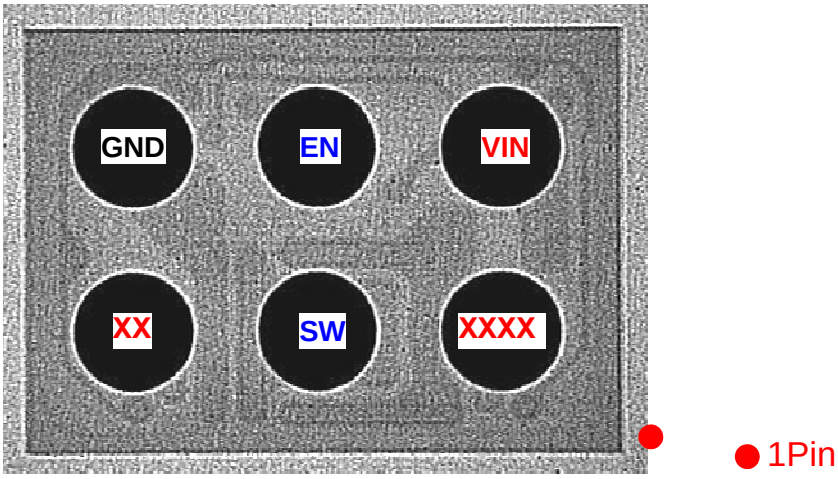
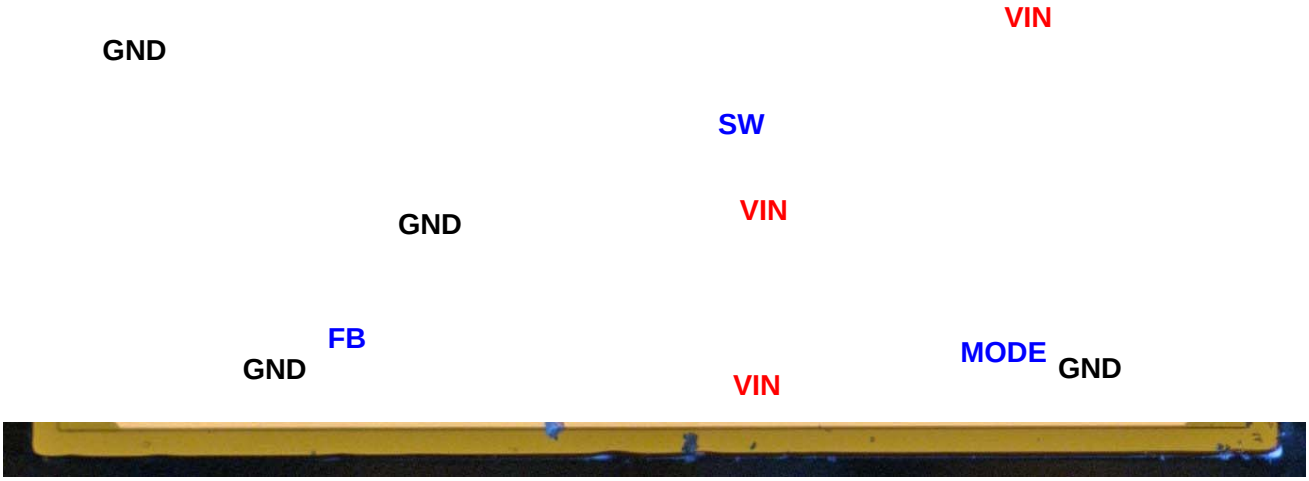


Photo.4-2 Pin Assignment (X-Ray)

Die photo was partially removed form Sample Report

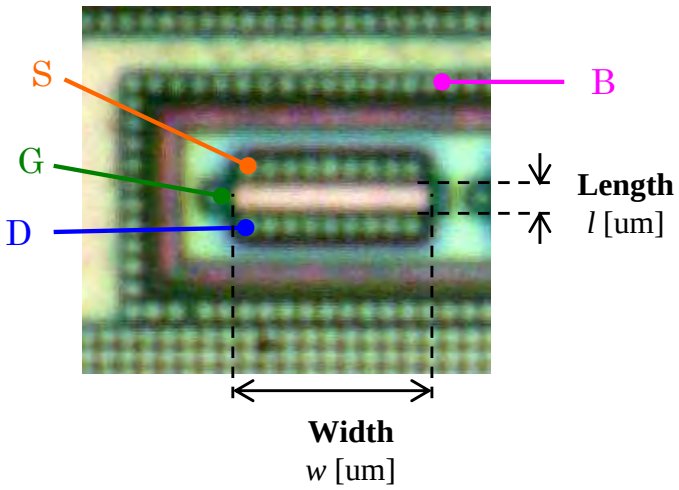


3Metal Layer

Photo.4-3 Pin Assignment (Chip Overview)

Elements

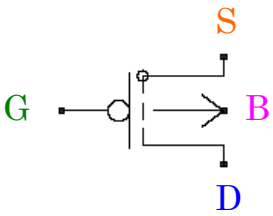
Layout



Cell Name (4 terminal)	Symbol	Cell Name (3 terminal)	Symbol

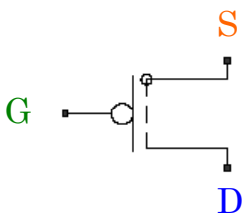
[PMOS]

mfetp4-1



M*n*
W=*w* u
L=*l* u
M=*m*
mfetp4-1

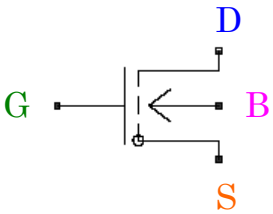
mfetp3-1



M*n*
W=*w* u
L=*l* u
M=*m*
B=*body*
mfetp3-1

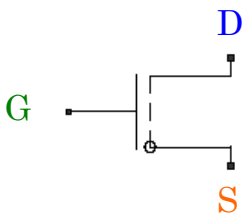
[NMOS]

mfetn4-1



M*n*
W=*w* u
L=*l* u
M=*m*
mfetn4-1

mfetn3-1

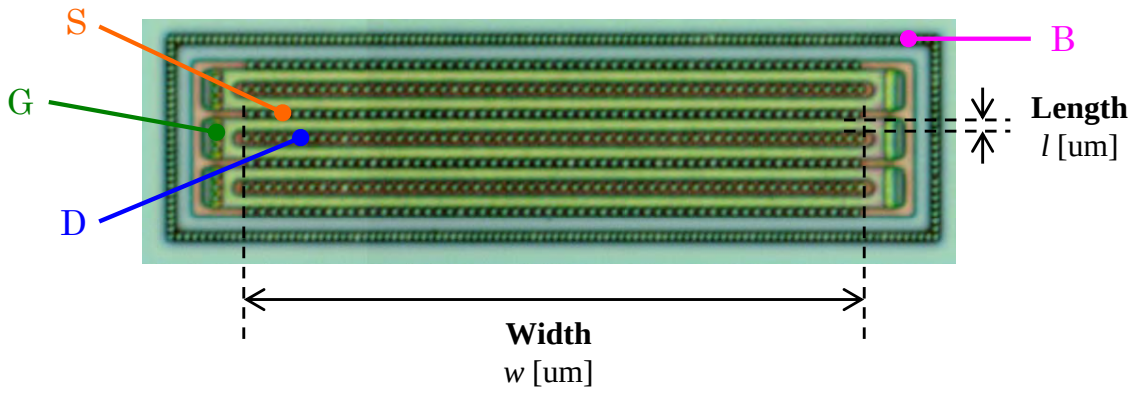


M*n*
W=*w* u
L=*l* u
M=*m*
B=*body*
mfetn3-1

n : element number
m : multiplier
body : body node

Photo.5-1 MOS Transistor1

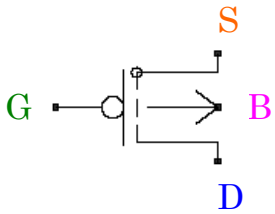
Layout



Cell Name (4 terminal)	Symbol	Cell Name (3 terminal)	Symbol

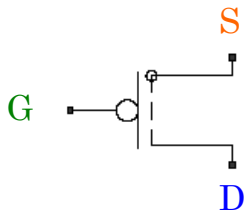
[PMOS]

mfetp4-2



M*n*
W=*w* u
L=*l* u
M=*m*
mfetp4-2

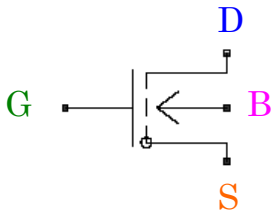
mfetp3-2



M*n*
W=*w* u
L=*l* u
M=*m*
B=*body*
mfetp3-2

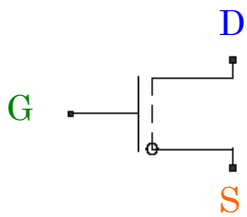
[NMOS]

mfetn4-2



M*n*
W=*w* u
L=*l* u
M=*m*
mfetn4-2

mfetn3-2

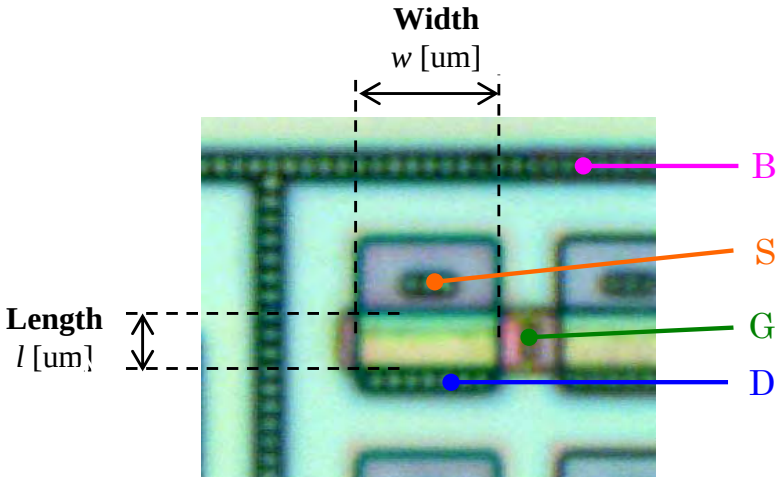


M*n*
W=*w* u
L=*l* u
M=*m*
B=*body*
mfetn3-2

n : element number
m : multiplier
body : body node

Photo.5-2 MOS Transistor2

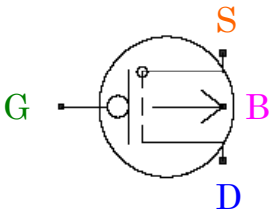
Layout



Cell Name (4 terminal)	Symbol	Cell Name (3 terminal)	Symbol

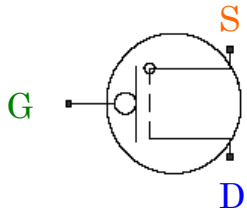
[PMOS]

mfetp4-h1



M*n*
W=*w* u
L=*l* u
M=*m*
mfetp4-h1

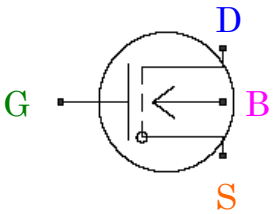
mfetp3-h1



M*n*
W=*w* u
L=*l* u
M=*m*
B=*body*
mfetp3-h1

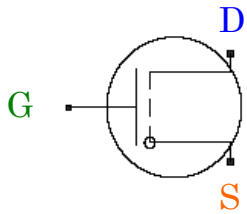
[NMOS]

mfetn4-h1



M*n*
W=*w* u
L=*l* u
M=*m*
mfetn4-h1

mfetn3-h1

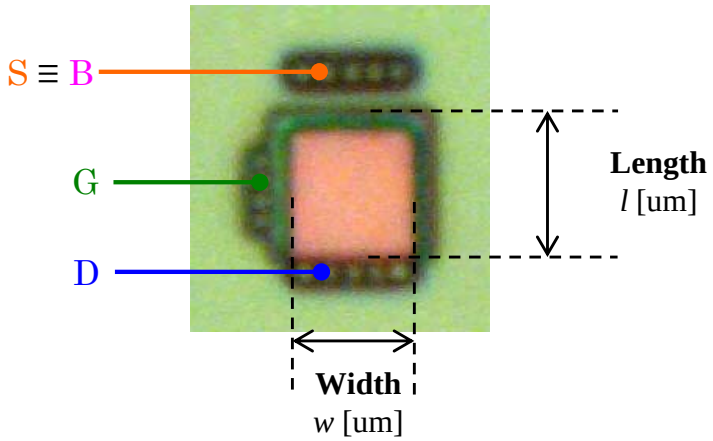


M*n*
W=*w* u
L=*l* u
M=*m*
B=*body*
mfetn3-h1

n : element number
m : multiplier
body : body node

Photo.5-3 HV-MOS Transistor1

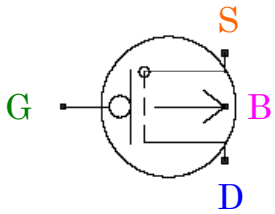
Layout



Cell Name (4 terminal)	Symbol	Cell Name (3 terminal)	Symbol

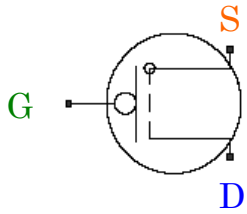
[PMOS]

mfetp4-h2



M*n*
W=*w* u
L=*l* u
M=*m*
mfetp4-h2

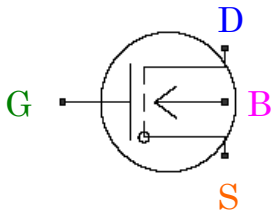
mfetp3-h2



M*n*
W=*w* u
L=*l* u
M=*m*
B=*body*
Mfetp3-h2

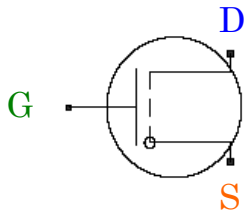
[NMOS]

mfetn4-h2



M*n*
W=*w* u
L=*l* u
M=*m*
Mfetn4-h2

mfetn3-h2

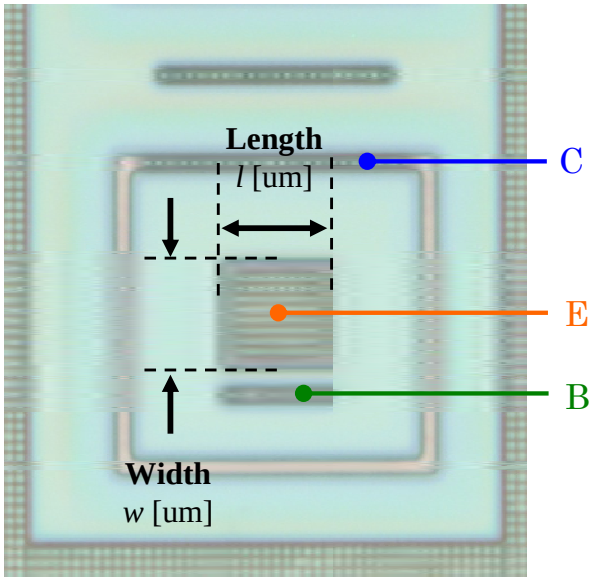


M*n*
W=*w* u
L=*l* u
M=*m*
B=*body*
Mfetn3-h2

n : element number
m : multiplier
body : body node

Photo.5-4 HV-MOS Transistor2

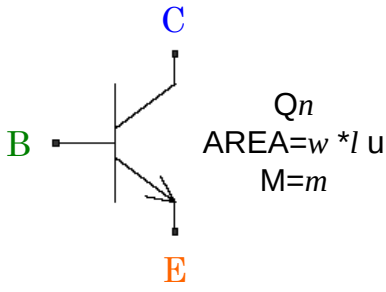
Layout



Cell Name

bjtn-1

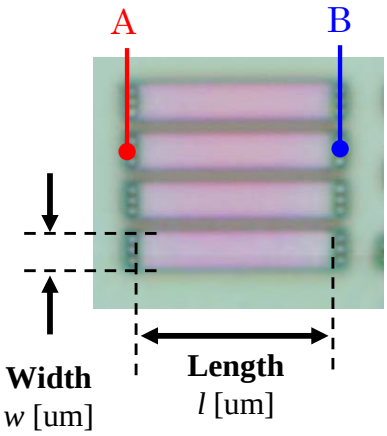
Symbol



n : element number
m : multiplier

Photo.5-5 Bipolar Transistor

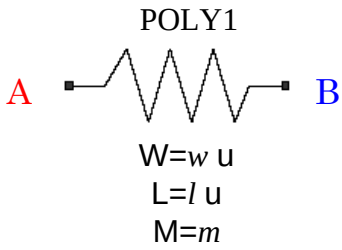
Layout



Cell Name

res1

Symbol



m : multiplier

Photo.5-6 Resistor1

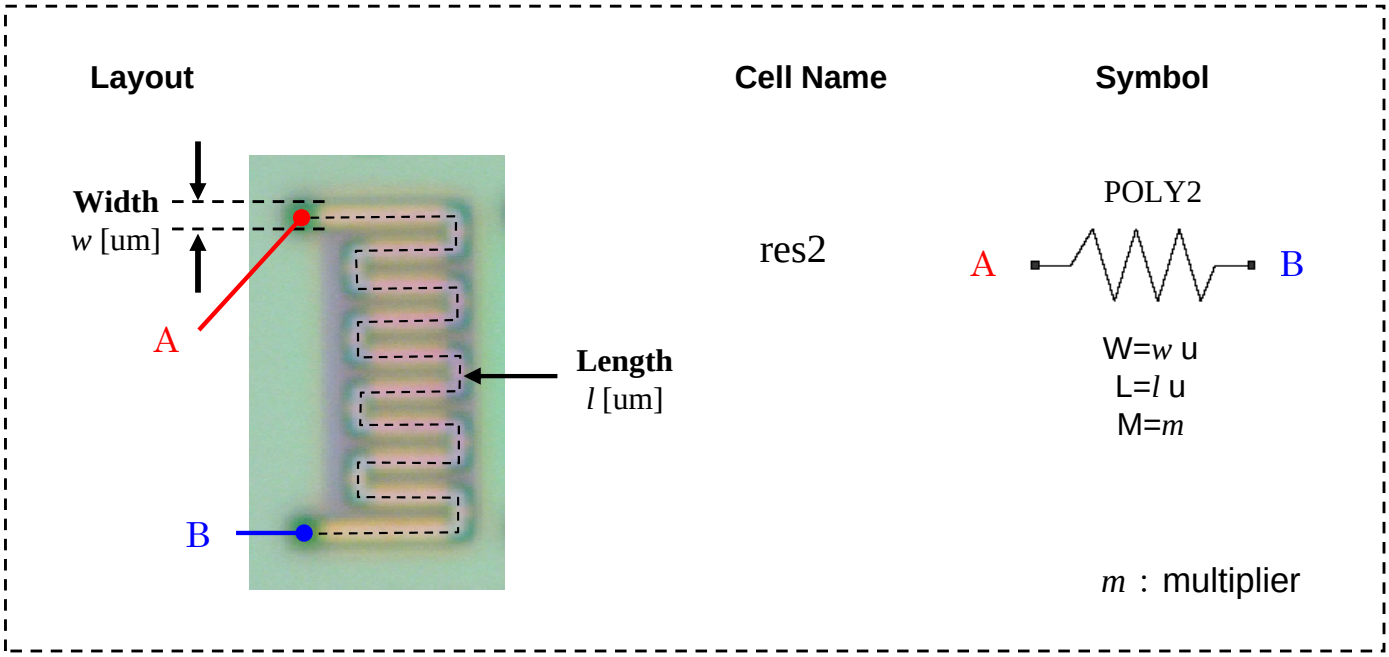


Photo.5-7 Resistor2

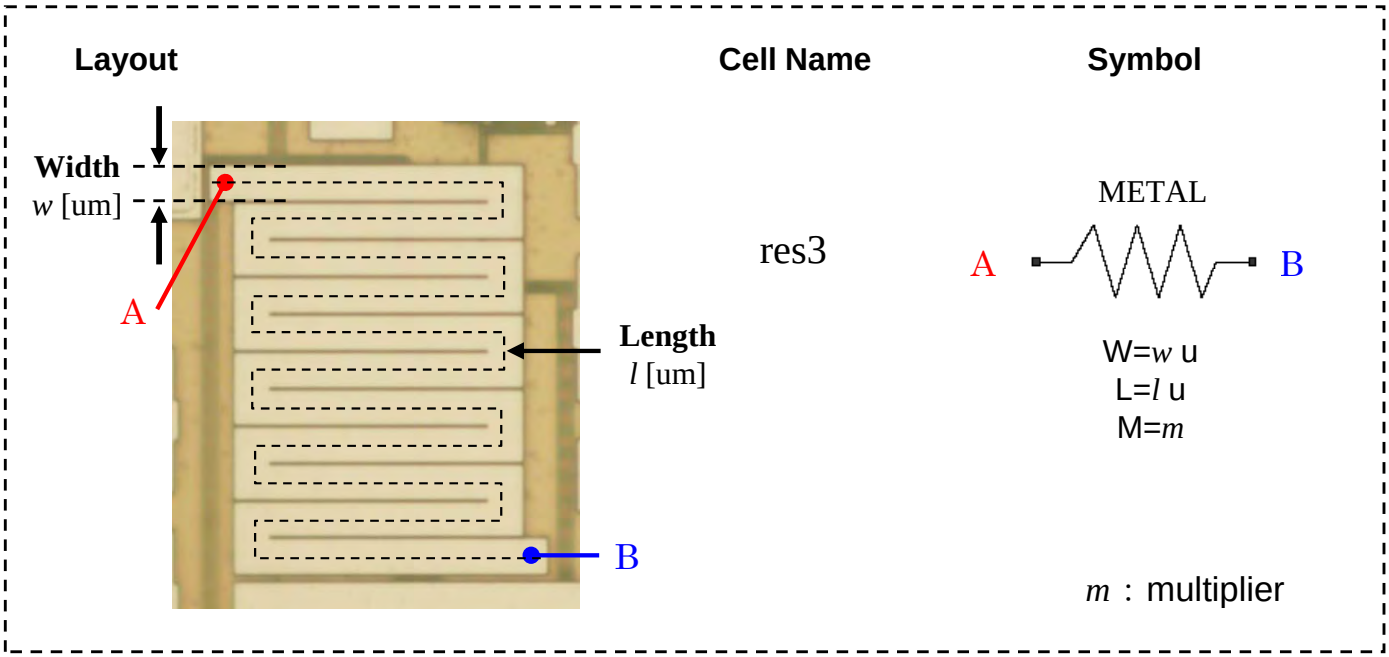


Photo.5-8 Resistor3

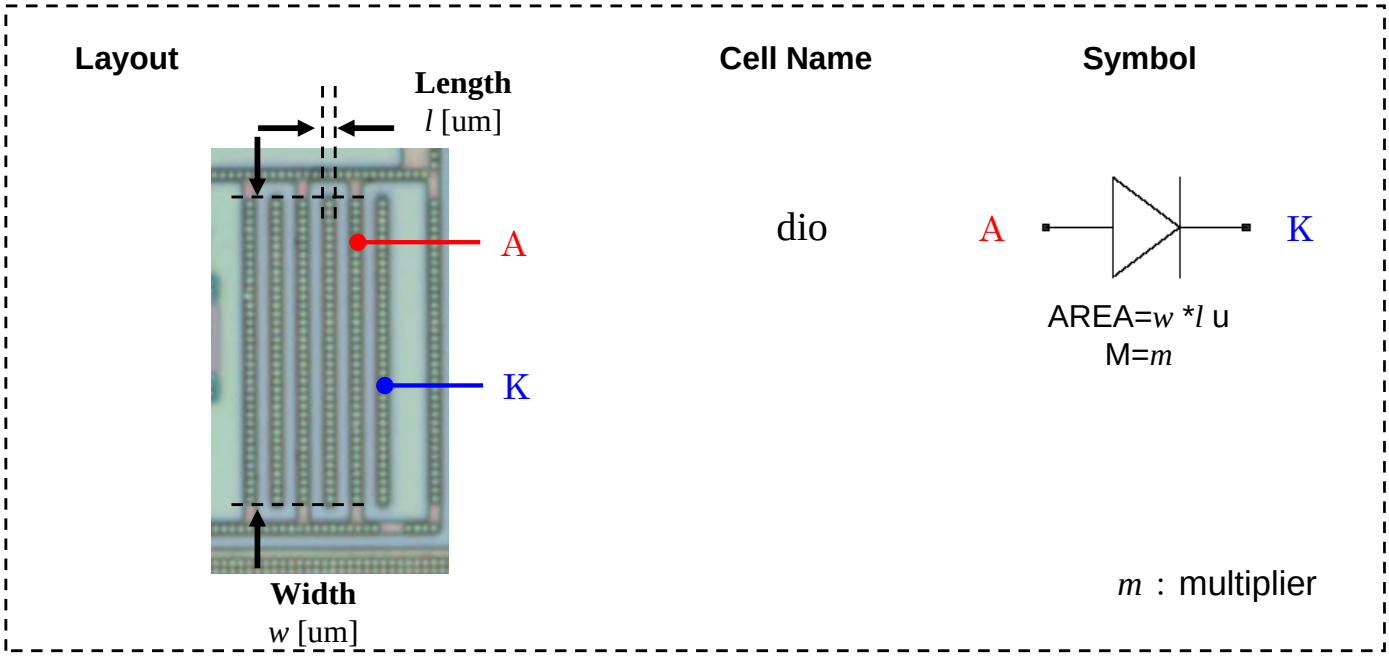


Photo.5-9 Diode

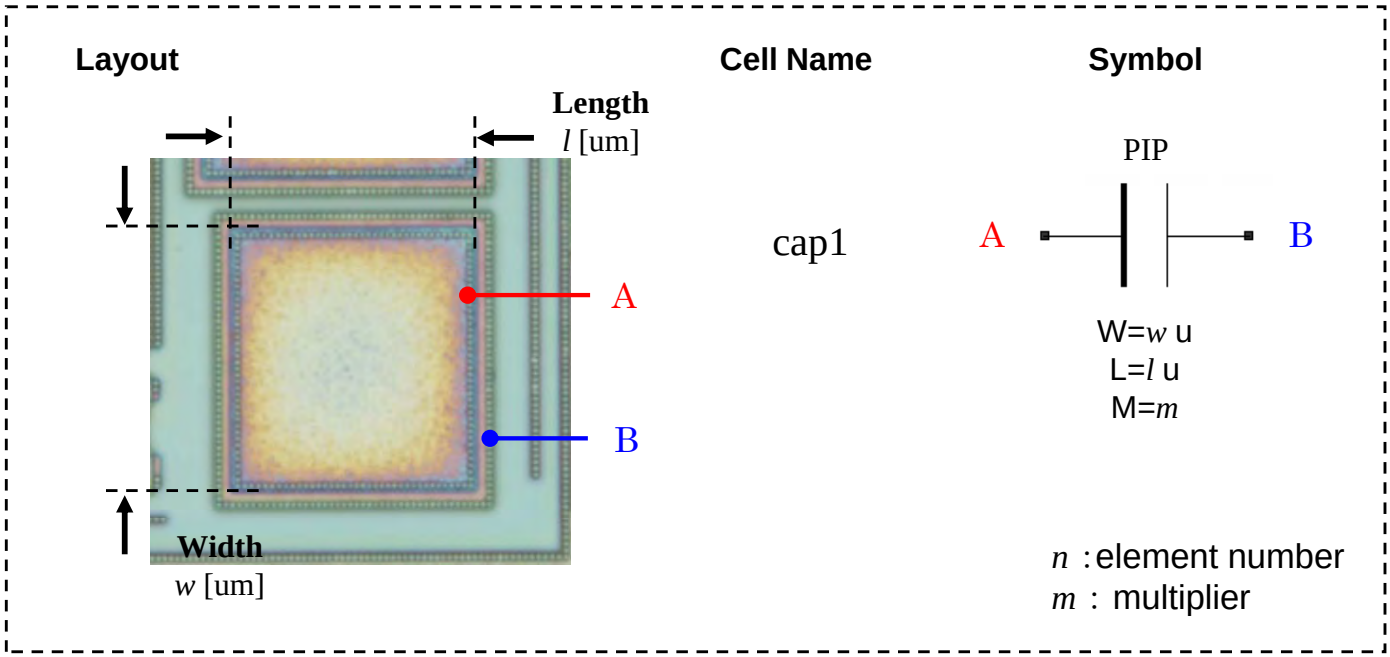


Photo.5-10 Capacitor1

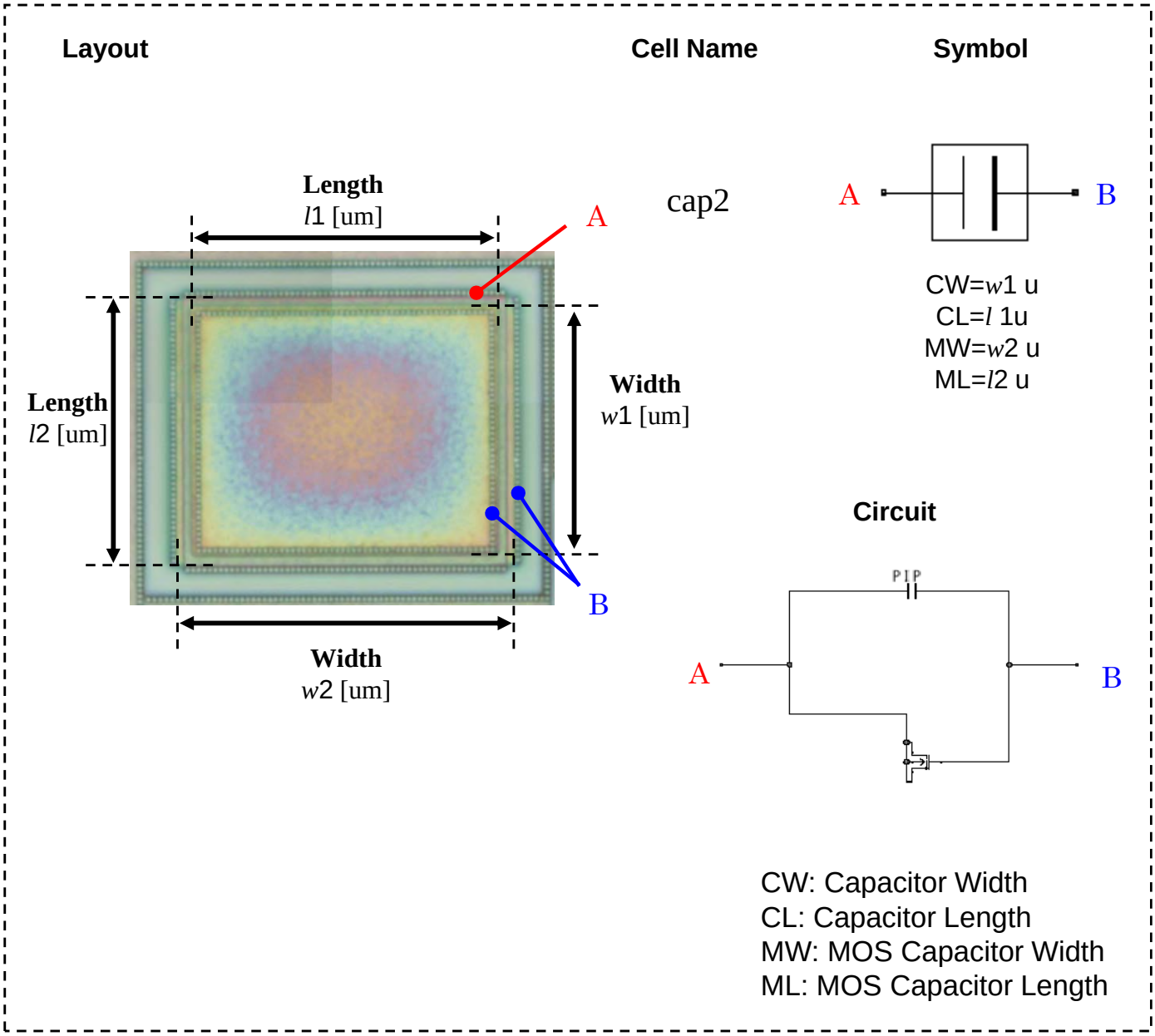
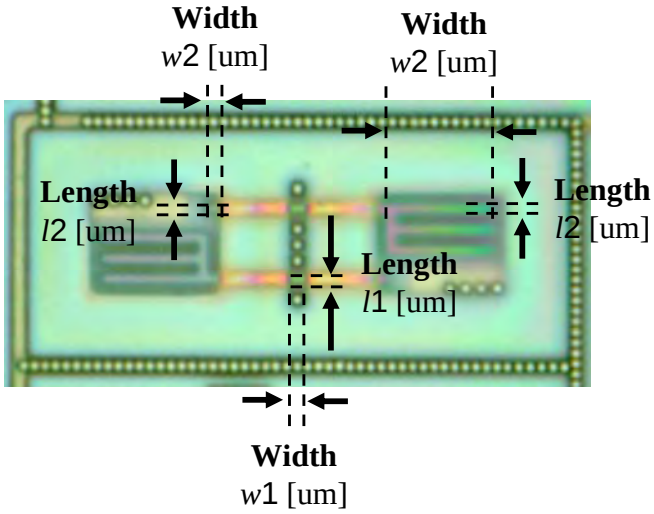


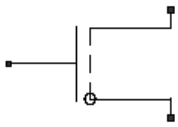
Photo.5-11 Capacitor2

Layout



cell name **symbol**

mfetn3-1



M*n*
W=*w*1 u
L=*l*1 u
M=*m*
B=*body*
mfetn3-1

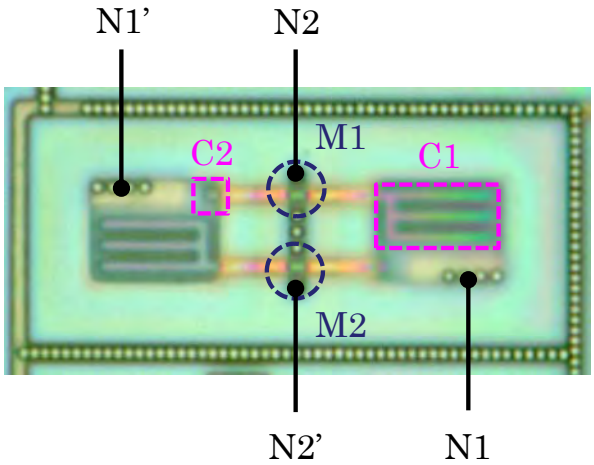
cap3

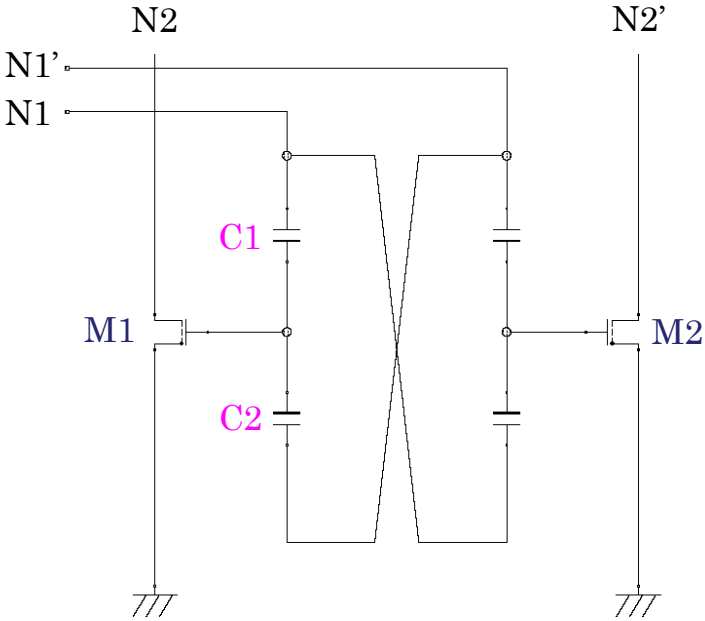
PID

W=*w2* u
L=*l2* u
M=*m*

n : element number
m : multiplier
body : body node

Circuit





C1:Control Gate
C2:Tunnel Area

Photo.5-12 EEPROM

Analysis Area Die photo was partially removed form Sample Report

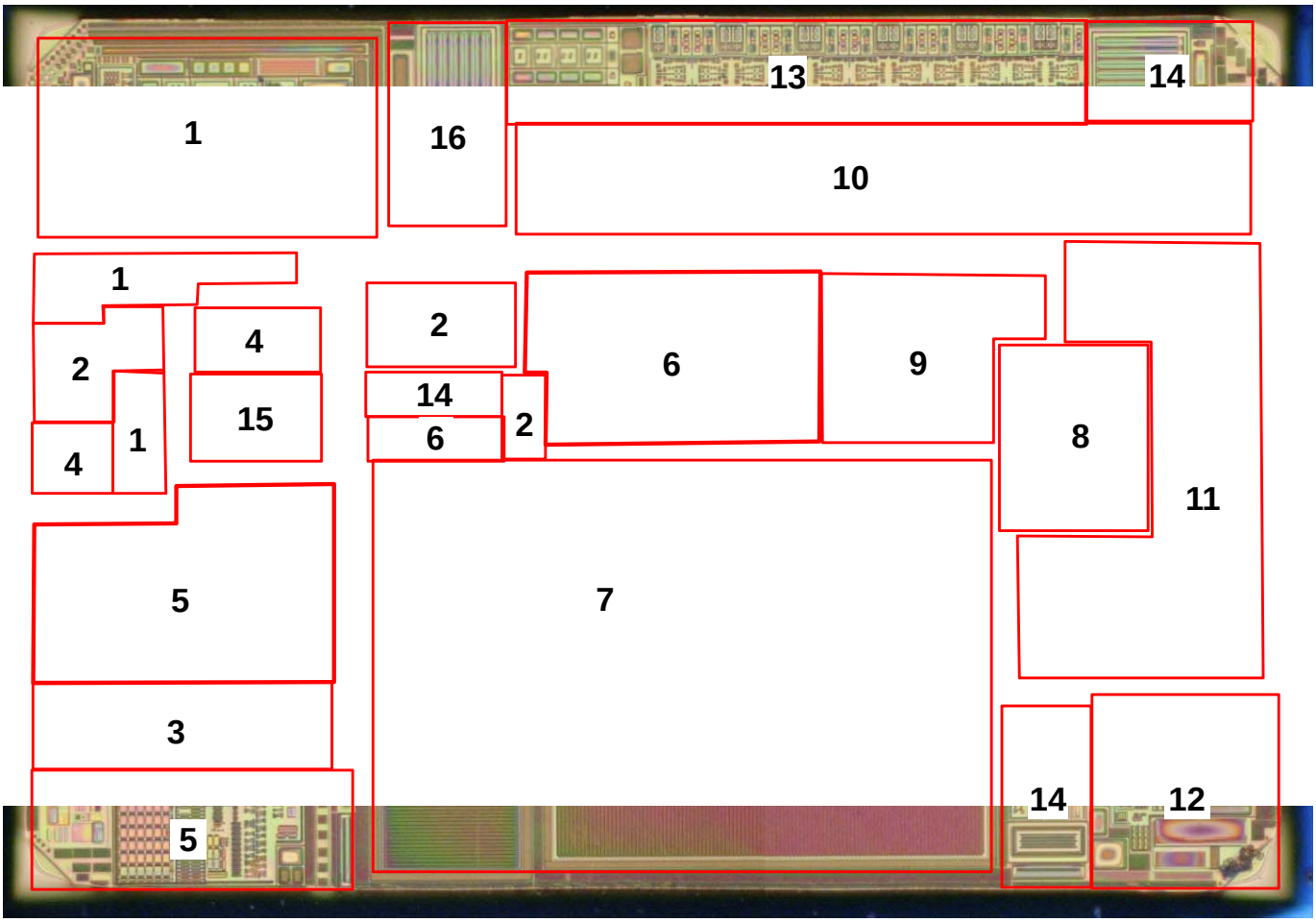


Photo.6 Analysis Area

Table2 Function

No.	Function	Fig.
1	Band-Gap and Bias Supply	Fig.2
2	UVLO Thermal Shutdown	Fig.3
3	FB Voltage Divider	Fig.4
4	PFM Comparator Block	Fig.5
5	PWM Comparator Block	Fig.6
6	Driver Control	Fig.7
7	Output Driver	Fig.8
8	Current Limit Detect	Fig.9
9	Negative Inductor Current Detect	Fig.10
10	Control Logic	Fig.11
11	Frequency Control	Fig.12
12	Oscillator	Fig.13
13	EEPROM Block	Fig.14
14	MODE Input Circuit	Fig.15
15	Soft Start	Fig.16
16	EN Input Circuit	Fig.17

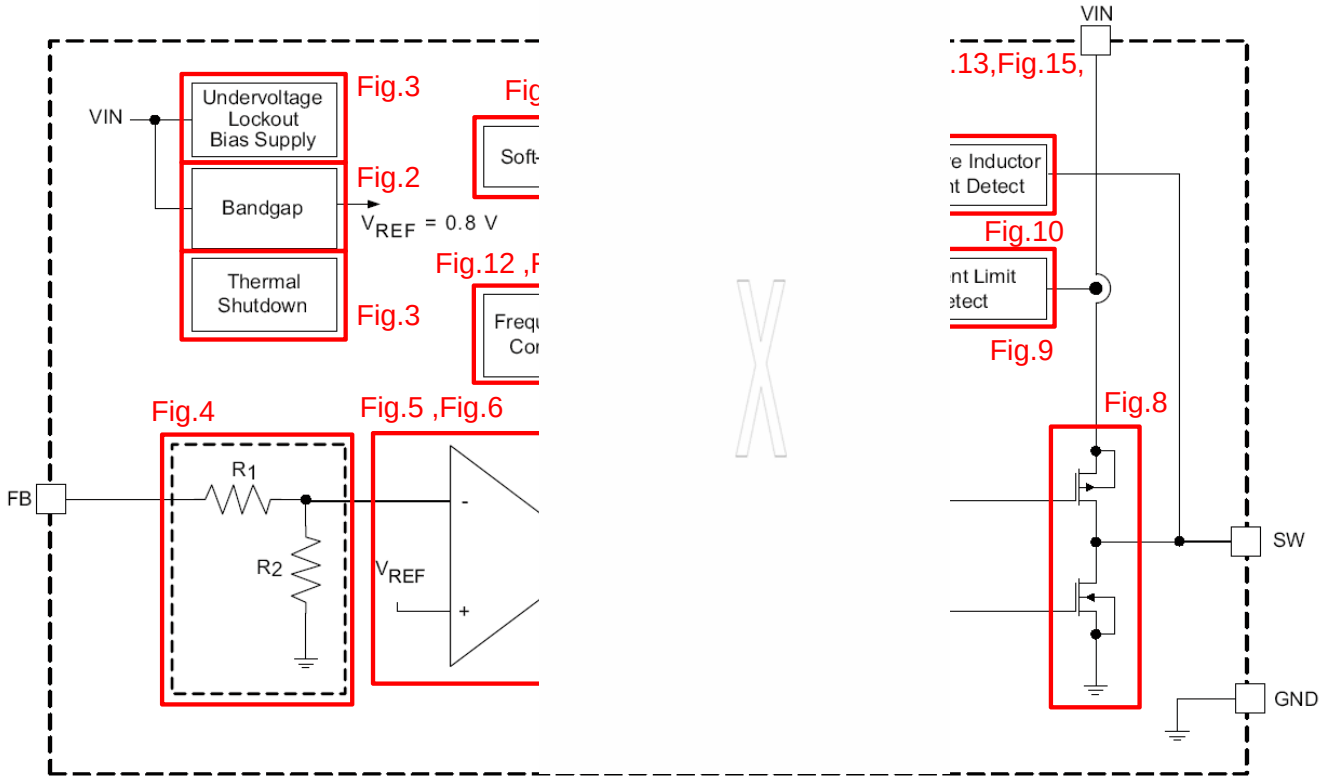
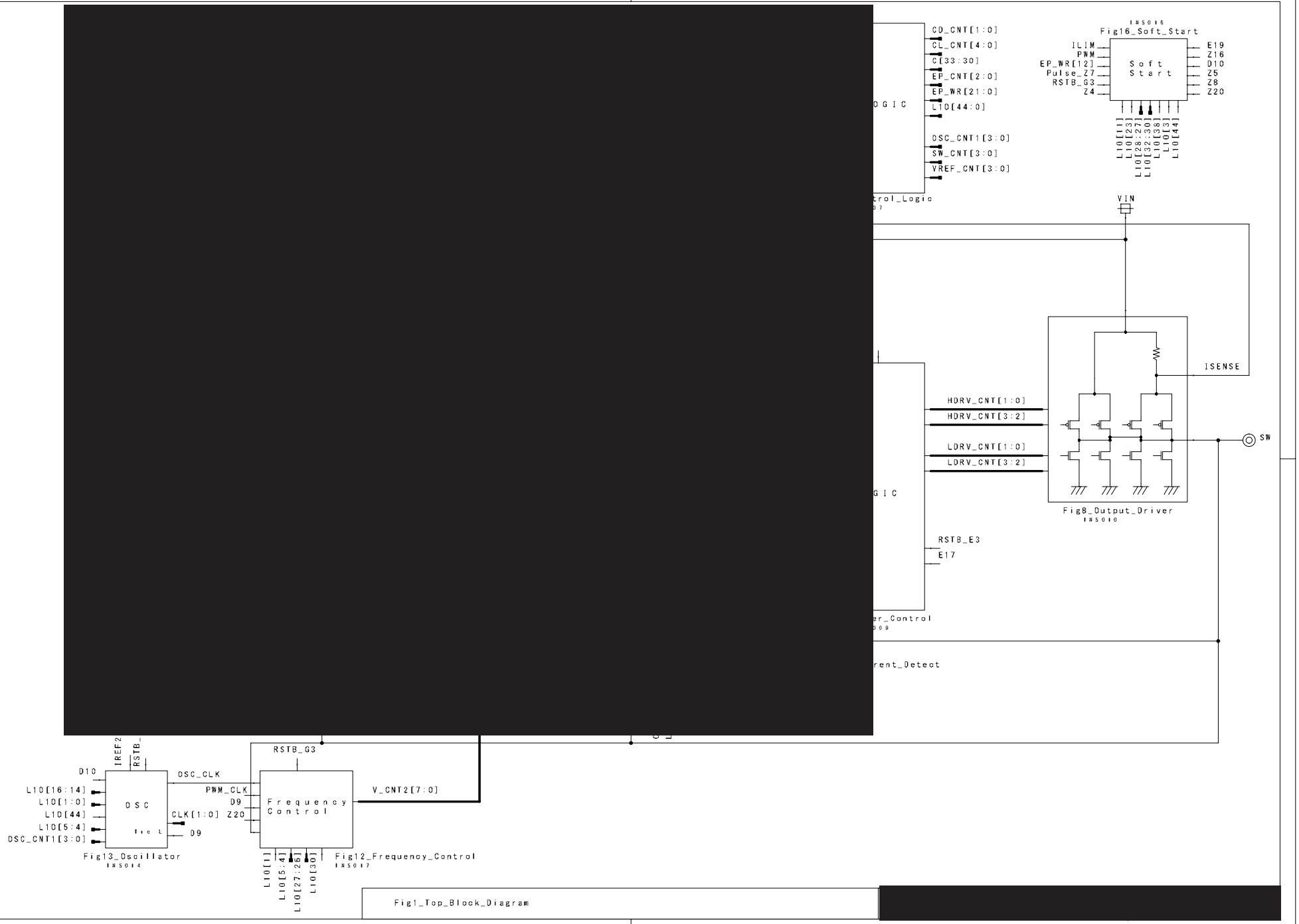


Fig.0 Functional Block Diagram


CD_CNT[1:0]
CL_CNT[4:0]
C[33:30]
EP_CNT[2:0]
EP_WR[21:0]
L10[44:0]
OSC_CNT1[3:0]
SW_CNT[3:0]
VREF_CNT[3:0]
Fig16_Soft_Start
ILIM
PWM
EP_WR[12]
Pulse_Z7
RSTB_G3
Z4
Soft Start
E19
Z16
D10
Z5
Z8
Z20
VIN
ISENSE
HDRV_CNT[1:0]
HDRV_CNT[3:2]
LDRV_CNT[1:0]
LDRV_CNT[3:2]
SW
Fig8_Output_Driver
RSTB_E3
E17
RSTB_G3
D10
L10[16:14]
L10[1:0]
L10[44]
L10[5:4]
OSC_CNT1[3:0]
OSC
OSC_CLK
PWM_CLK
D9
CLK[1:0]
Z20
D9
Frequency Control
V_CNT2[7:0]
Fig13_Oscillator
Fig12_Frequency_Control
L10[1]
L10[5:4]
L10[27:26]
L10[30]
Fig1_Top_Block_Diagram

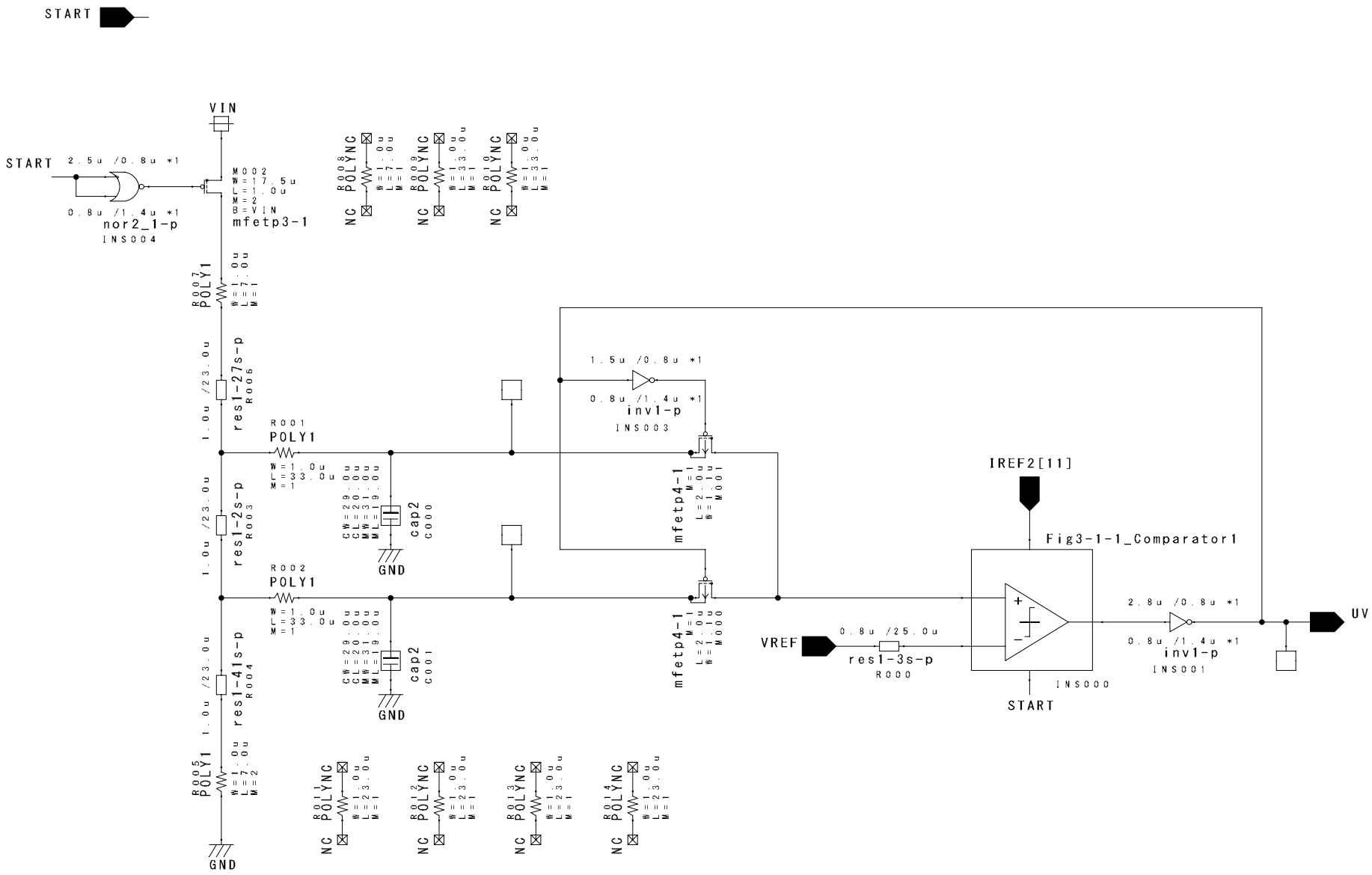


Fig3-1_Under_Voltage_Detector

NOTE000

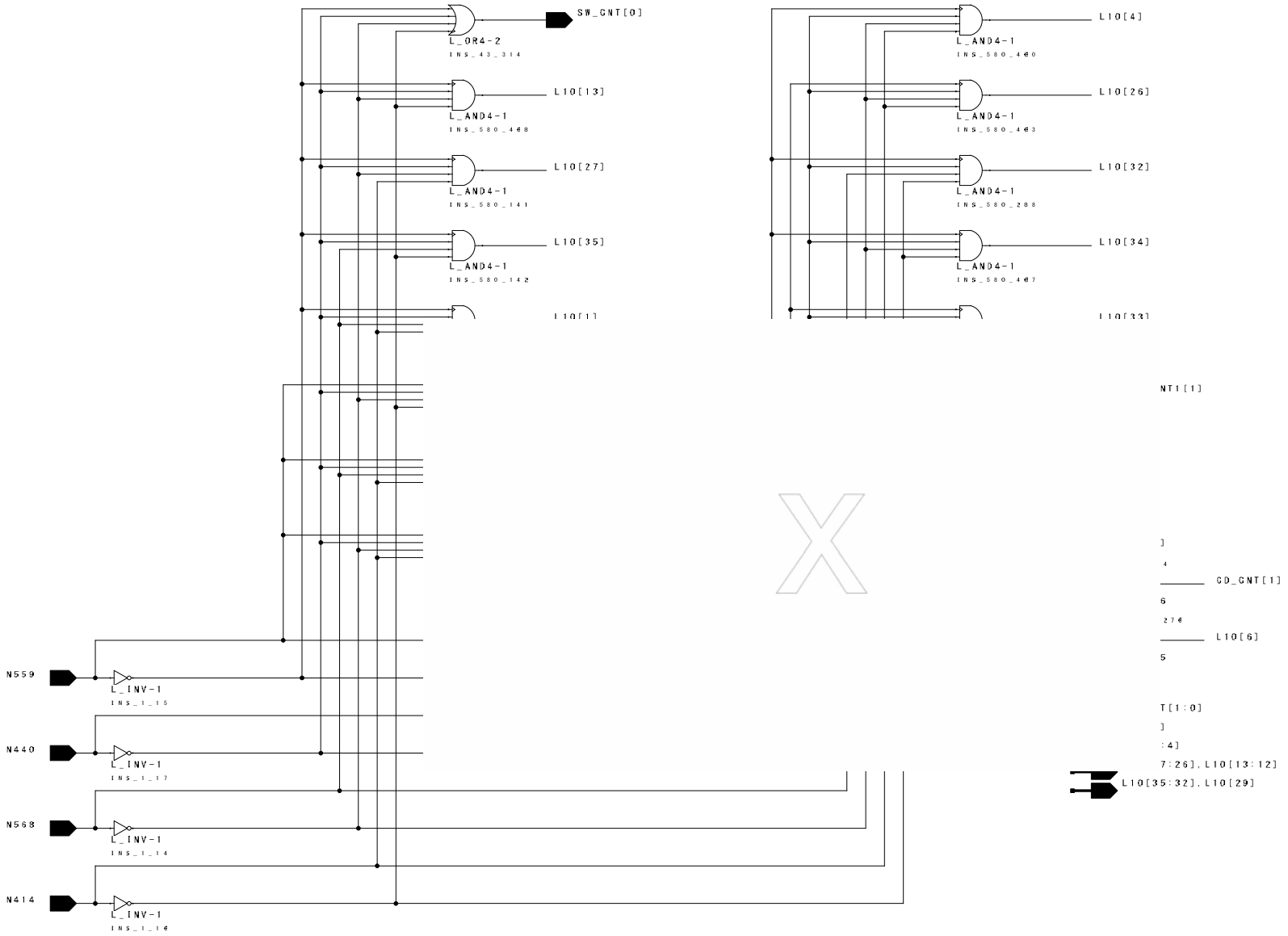
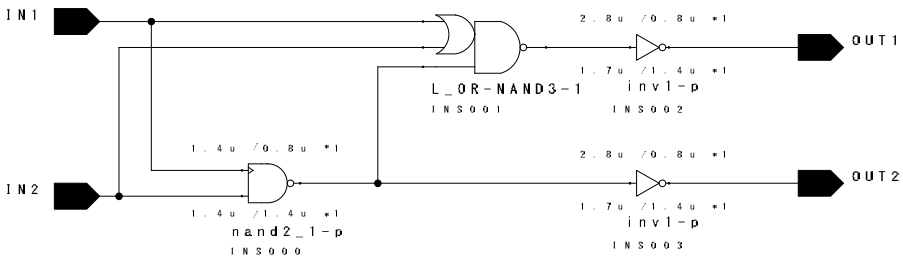


Fig11-1-3-9_L1_Decoder

[redacted]



LOGIC-cell-3

[redacted]

NOTE000